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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,243	12/05/2001	Chia-Hsing Yu	VIAP0010USA	8325

27765 7590 05/20/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	6

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,243	YU ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 is/are rejected.

7)☒ Claim(s) 2-15 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Original claims 1-15 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gebara et al., U.S. Patent No. 6,035,407 ("Gebara"), in view of Philips Semiconductors, "PCA9559 System Management ICs", 2000 ("Philips").

As per claim 1, Gebara teaches an integrated circuit adapted for supporting a processor, the integrated circuit (Fig. 11, PLD 112) comprising:

an input line for indicating a type of said processor (Col. 7, lines 43-62, an input line for PLD 112 to read CPU-ID 114; Fig. 15, step 126);

a plurality of input lines for indicating a programmable core voltage requested by said processor (Fig. 15, step 124; Col. 8, lines 42-45, input lines for designed core voltage specified by processor's VID pins);

a plurality of input lines for indicating a default core voltage of said processor (Fig. 15, step 128; Col. 2, lines 15-23; Col. 7, lines 43-62, since the designed core voltage is multi-bit, so must the actual core voltage);

a plurality of input lines for indicating a processor operating frequency (Col. 6, lines 22-39, processor provides multi-bit frequency identification output (FIDO); Fig. 10A, input lines for PLD 94 to receive FIDO; Col. 7, lines 38-42, PLD 94 is same as PLD 112); and

a plurality of output lines for providing a Frequency-Identification value, said Frequency-Identification value corresponding to an operating frequency of said processor (Col. 7, lines 26-32, output lines to programmable oscillator 96).

However, Gebara does not expressly teach details such as a plurality of power signal input lines. Philips teaches a plurality of power signal lines to an integrated chip (Figure, positive rail voltage Vcc and ground GND). Gebara and Philips are analogous because they involve integrated circuits for setting computer processor voltage and frequency. At the time of the invention, it would have been obvious to one of ordinary skill in that art to apply Philips power signal lines to Gebara's integrated circuit.

Gebara further does not expressly teach a Frequency-Identification value to a North Bridge chipset or a South Bridge chipset. Philips teaches interfacing a north bridge or south bridge chipset to configure processor frequency (Application 1).

Though Gebara does not expressly teach a plurality of output lines for overriding an internal Frequency-Identification code of said processor, Gebara's voltage override method (Col. 8, lines 10-30) may be applied to override frequency for powersaving or overclocking (Philips, Application 2). In order to implement powersaving, an additional input line for indicating a sleep state of said processor would be required.

Allowable Subject Matter

3. Claims 2-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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May 16, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100